



Synchronization and Interconnect in Multi-Clock Domain Systems-on-Chips

5-7 August 2009

Presenter: Professor Ran Ginosar, Technion, Israel
Holiday Inn, Potts Point NSW

The course will be conducted from 9.00am to 5.00pm. Morning tea will be available at approximately 10.00am to 10.30am, lunch from 12.30pm to 1.30pm and afternoon tea at approximately 3.00pm to 3.30pm.

Registration Fee: AU\$1980
(incl. GST)

Early Bird Fee: AU\$ 1683
(incl. GST) – register by May 1st.

Group and PhD student discounts available. Please enquire.

How to Register

To register fill out the registration form (overleaf) and

- fax it to +61-8-8343-8711

or

- scan and email it to industryeducation@nicta.com.au

Cancellation Policy

At least **4 weeks** notice is required for cancellation of a place in a course for full reimbursement. If cancellation is later than 4 weeks then the place can either be given to another person or the registrant can be provided with a credit towards other NICTA training.

For details of further courses please see our web site: www.nicta.com.au/short_courses or contact NICTA Industry Education Manager.

About this Course

This **3-day** course teaches the science, engineering and art of synchronization. We define the problems, survey existing solutions, study the best designs, and learn how to select the better synchronizer for each purpose. We review clocking in digital chips, study the required theoretical basics, learn how to understand synchronization problems, identify them, create reliable solutions, and verify their correctness. We consider SoC / ASIC and FPGA, mostly at the logical level. Implications on physical design are briefly reviewed. We also review voltage domains, power gating, voltage scaling and their effect on clock domains and synchronization.

Target Audience: VLSI/ASIC/SoC/FPGA design engineers, architects and managers engaged in the design of advanced SoC; VLSI/ASIC/SoC/FPGA CAD engineers and developers; Academic researchers, university professors, and graduate students interested in advanced SoC design.

Assumed Knowledge: Basic knowledge of digital VLSI/ASIC/FPGA design is assumed. Prior exposure to issues and pitfalls of synchronization is an advantage, but neither such exposure nor prior knowledge of synchronization is necessary. General background in electrical or computer engineering is useful.

Brief Course Outline

Day 1. We review the synchronization problem, examine conventional clock distribution networks and consider the issues faced while designing them. Delay variations, technology trends and scaling are discussed. Methods of overcoming some clocking and timing problems are reviewed. Synchronization failures and metastability are studied closely, including basics of latches, flip-flops and the importance of race-free design.

Day 2. We study the various available synchronizers and learn when it is best to apply each one. Common synchronization errors are discussed and presented, so that we can avoid them. Commercial EDA tools for formal verification of synchronizers are examined and verification with more standard tools is discussed.

Day 3. We consider aggressive and complex synchronizers for communications between two related clock domains, whose frequencies are the same or multiples of each other. Methods for long on-chip interconnects between unrelated clock domains are reviewed. We conclude with Globally Asynchronous Locally Synchronous (GALS) SoCs and study novel and efficient approaches to multiple clock domains that may be required for SoCs using advanced processes.

Please visit [the course web page](#) for more information on the topics covered in the course.

About the Presenter



Ran Ginosar, PhD, Head of the VLSI Systems Research Center and Associate Professor, Electrical Engineering and Computer Science departments at the Technion-Israel Institute of Technology.

Professor Ginosar has published numerous papers and his inventions have resulted in a large number of patents. His research interests include VLSI architecture, asynchronous logic and synchronization, electronic imaging, networks-on-chip, many-core architecture and bio-chips. He is presently engaged in research of multiple aspects of synchronization, partly in collaboration with industry. He has taught a number of industrial courses on synchronization, on-chip interconnect and multiple clock domain SoC since 2003.

About NICTA and Short Course Program

National ICT Australia (NICTA) is Australia's ICT Centre of Excellence and was established to drive innovation through high quality research, research training and technology transfer. As a world-class research institute NICTA uniquely combines excellence in research, education, commercialisation and collaboration. We are working to ensure that Australia is well placed to benefit from the significant opportunities that ICT research delivers.

NICTA is funded by the Australian Government as represented by the Department of Communications, Information Technology and the Arts and the Australian Research Council through *Backing Australia's Ability* and the ICT Centre of Excellence program. NICTA members are the Australian Capital Territory Government, the New South Wales Government, the University of New South Wales and the Australian National University.

NICTA short courses offer scientists, engineers and managers technical training with a leading edge in areas such as telecommunications, transport, security, defence, logistics, e-government, mining, finance and biotechnology.

There will be ample opportunities for discussion and questions and answers. Morning and afternoon tea/coffee and a light lunch will be provided. Extensive workshop materials will be made available to participants.

How to register

Please complete the registration form below and

- Fax it to +61-8-8343-8711 or
- Scan and email it to industryeducation@nicta.com.au

Send the form as soon as possible to secure your place.

For further information please contact
Anne-Marie Eliseo
Industry Education Manager
Telephone: +61-8-8343-8710
Email: anne-marie.eliseo@nicta.com.au

Registration Form and Tax Invoice* ABN 62 102 206 173

*Upon completion of this form, including the relevant payment, this form will become a Tax Invoice.

Please register me for Synchronization and Interconnect in Multi-Clock Domain Systems-on-Chips on 5-7 August 2009.

PLEASE PRINT

Date: _____

Title: _____ First Name: _____ Surname: _____

Position: _____ Organisation/Division: _____

Postal Address: _____

Telephone No: _____ Facsimile No: _____ Email: _____

Dietary preference: _____

Course Fees: Early Bird Fee: AU\$1683 (incl. GST)
(Register before **May 1st, 2009.**)

Regular Fee: AU\$1980 (incl. GST)
(Register before **Jul 22nd, 2009.**)

Method of Payment (please tick below):

Cheque (payable to National ICT Australia Ltd)

Forward the cheque and a copy of THIS registration form to:

Anne-Marie Eliseo, Industry Education Manager, NICTA, Innovation House, First Avenue, Mawson Lakes SA 5095, Australia.

Credit Card: Credit Card No.: _____ Expiry Date: _____

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Electronic Funds Transfer

Please advise by email to Annette Van Bramer
annette.vanbramer@nicta.com.au
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- Send an email to comments@nicta.com.au or
- Phone NICTA's Industry Education Manager on +61 8 8343 8710.