

2x2 MIMO Testbed for Dual 2.4GHz/5GHz Band

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Abstract — The paper describes a Multiple Input Multiple Output communication testbed for operation in a dual 2.4GHz/5GHz band, which is under development at the University of Queensland. This advanced testing equipment makes use of Field Programmable Gate Array technology for fast processing of the baseband signals. Its RF modules include commercially available RF transceiver chips and in-house developed antennas. Using a 100Mbit Ethernet network connection and a web browser, the estimated channel matrices and received and decoded signal constellations can be visualized in quasi real-time on a personal computer.

1 INTRODUCTION

Multiple Input Multiple Output (MIMO) signal transmission is an emerging cost-effective technology that offers significant improvements to data throughput and reliability of wireless systems in non-line-of-sight environments [1, 2]. In contrast to the traditional single transmit single receive antenna wireless system (also known as SISO), the MIMO system utilizes multiple element antennas (MEAs) both on transmit (Tx) and receive (Rx) sides of the communication link.

Investigating properties of the actual channels and devising suitable signal transmission schemes for MIMO has been the subject of many recent world-wide research activities [2]. From these investigations, it has been established that in order to fully test the capabilities of MIMO under real conditions, a suitable demonstrating system, also known as testbed, is required.

Current literature shows quite an extensive number of MIMO demonstrator/testbeds. The works reported in [3–11] give a good representation of the current activities in this area. The reported testbeds can be classified into two main categories, *online* and *offline*. An *online* testbed is able to fully process the input and output data streams in real-time, as they are produced. An *offline* one does not process continuously an incoming data in real-time and so it saves it for future processing.

An overview of the work described in [3–11] shows that MIMO testbeds have gone through a number of technological changes. Initially, they used a digital capture card, which enabled *offline* data processing on a PC. In order to accelerate

the processing of the captured data, the next generation of testbeds utilized the high speed digital signal processors (DSP). The shortfall of the DSP approach is that it requires higher clock rates as the design complexity scales with additional antennas or more signal processing. This shortfall can be overcome by using Application Specific Integrated Circuits (ASIC) or Field Programmable Gate Arrays (FPGA), which perform signal processing in parallel. FPGA offers performance similar to the ASIC based designs, except that it is reconfigurable, and hence suitable for the rapid prototyping of new MIMO transmission schemes.

This paper reports on the design and development of a 2x2 MIMO demonstrator at the University of Queensland (UQ). It uses a FPGA board for processing of a baseband signal and an RF board with commercial transceiver chips and in-house developed antennas for operation at 2.4GHz and 5GHz bands. The system offers a quasi-real-time visualization of signal transmission and thus a convenient method of verifying its performance. At present, it employs QPSK signal modulation and the Alamouti coding scheme. With respect to channel estimation it applies both the training sequence and blind approach. The operation of this system is verified using a purpose built channel emulator.

2 SYSTEM DESCRIPTION

The concept of the system is shown in Fig. 1. This system includes a transmitter (Tx) and Receiver (Rx) each equipped with two antennas, separated by a wireless channel. The relationship between the Tx and Rx signals is given by (1).

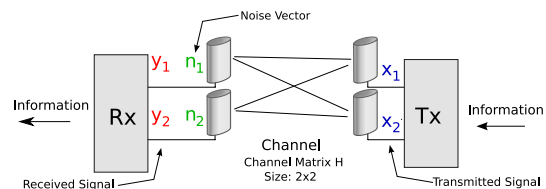


Figure 1: 2x2 MIMO system concept.

$$y = Hx + n \quad (1)$$

where H is the 2x2 complex channel matrix, x is the transmitted signal vector, y is the received signal vector, and n is the noise vector.

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The FPGA baseband signal processor is similar in concept to those described in [8,9]. With respect to the design of RF front-ends, the system shows similarities with the MIMO testbed presented in [6].

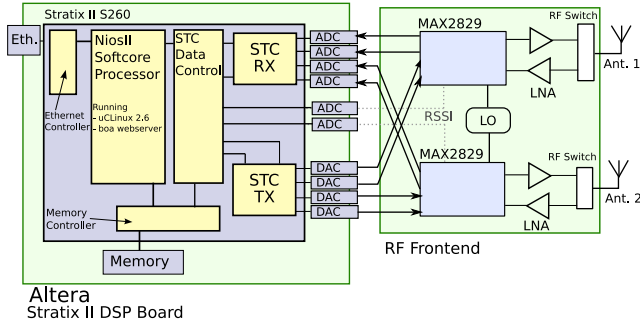


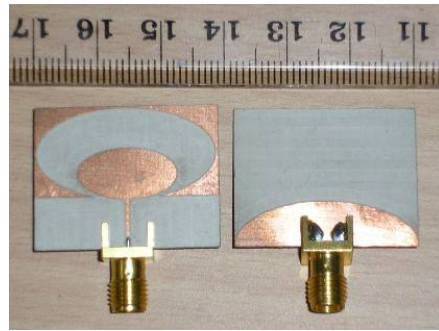
Figure 2: The block diagram of the complete 2x2 MIMO system.

As seen in Fig. 2, the UQ MIMO testbed includes two main modules, the baseband signal processor and the RF front end. The FPGA signal processing module is designed around the Altera Stratix II S260 chip. The RF front end module performing direct conversion between baseband and the 2.45GHz or 5GHz frequency bands employs the MAX2829 IC chip. The middle part between FPGA and RF front end is a set of analogue to digital (ADC) and digital to analogue (DAC) converters that operate on signals between the FPGA and the RF transmitter/receiver modules. They are capable to handle 125MSmp/sec. 12/14 bit signals. The currently chosen data rate is 3.125Mbps. In addition to the MAX2829 IC chip, amplifiers, switches and antennas are included in the RF module. For post processing of results and visualization, special buffers and a soft-core processor running uClinux for network connectivity is added. Visualization of results on PC is accomplished via networking using the embedded Ethernet controller. Fig. 3 shows photographs of these major system components, including planar monopole antennas and RF and baseband hardware forming the testbed.

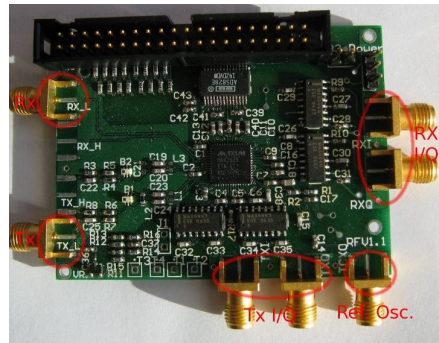
Details of major components of this system are described as follows.

2.1 Baseband Transmitter

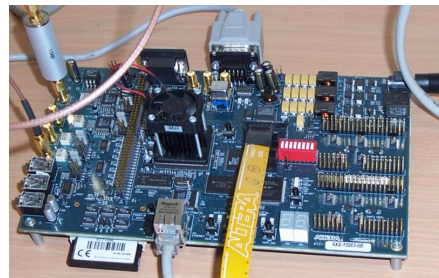
It takes the input bit stream and prefixes the training sequence to every packet. For each packet the data sequence is split between the two antennas, encoded using the Alamouti encoding scheme [12] and modulated using QPSK.



(a) wideband planar monopole antenna



(b) RF front-end board



(c) FPGA baseband processor board

Figure 3: Photographs of the developed subsystems.

2.2 Baseband Receiver

It has two modes of operation. The first involves the use and detection of the training sequence and the second concerns adapting the channel estimation using the new incoming data. This is performed by taking the I and Q signals for both receiving channels and performing a maximum likelihood (ML) decoding and estimation. The ML decoder and estimator run in parallel and are controlled by the STC scheduler. The two modes differ by what values are used for the ML estimator block.

2.3 Channel Emulator

This is responsible for generating the current channel matrix and white noise. We use two approaches to provide the channel matrix data. One

is based on the signal bounce scattering model [13]. The other one employs a set of channel matrices that are obtained from measurements in indoor environment using a vector network analyzer (VNA). The channel emulator is implemented in the time domain. The set of channel matrices are pre-generated and stored in a look-up table, and randomly selected at run time. By adjusting the period that a channel matrix remains constant, slow and block fading can be emulated. With respect to white noise, the noise data is pre-generated and stored in a table.

2.4 Coding and estimation algorithms

The Alamouti coding scheme involves a space time block which has a pair of symbols sent in the first block period, and then a modified version of these symbols in the second block period.

The channel matrix estimation and data decoding employs an algorithm, which is based on the maximum likelihood (ML) decoding and estimation technique [14]. In the testbed a semi-blind channel estimation algorithm, which involves the training mode and the adaptive mode, is applied. During the training mode, the known training sequence is used to estimate the channel. For purposes of synchronization the first 4 symbols of the training sequence are sent on only one antenna, to simplify the synchronization problem, like in a SIMO system. After this, an additional 28 symbols/14 blocks are sent using both antennas. Following the training sequence, the receiver enters an adaptive mode. In this mode, the received symbols are decoded using the previous valid channel matrix, and the result is quantized to the nearest correct symbol and used to estimate the new channel matrix. In order to reduce the effects of noise, the channel matrix used for the next iteration, is a weighted average of the old and new channel matrix estimations. The weighting ratio is between 1:8 and 1:32. Its choice depends on how big a change the previous and current estimations are from their previous values. The estimation which is less of a change is given a larger weight.

3 SYSTEM VERIFICATION

Verification of the 2x2 MIMO testbed operation is done separately with respect to RF module, antennas and baseband module. Most of the effort goes into the FPGA baseband module testing where the majority of signal processing takes place.

3.1 RF Module

The first form of verification involves checking the MAX chip is operating correctly. This involves powering it up and checking that the internal PLL

locks. After this the transmit path and receive path need to be tested separately. For the transmit path, a test signal with I and Q components is applied on the Tx I/Q inputs, and the TX_L or TX_H output is read on a spectrum analyzer. For the receive path an RF signal generator is used to form a 2.45GHz or 5GHz wave for the RX_L and RX_H inputs. The output is read on two channels, the Rx I/Q outputs.

3.2 Antennas

The planar monopoles are designed and developed assuming Rogers RT6010LM substrate, which features relative permittivity of 10.2 and a loss tangent of 0.0023, 0.64mm thickness plus $17\mu\text{m}$ thick conductive coating. The antenna shown in Fig. 3(a) has dimensions $20\text{mm} \times 30\text{mm}$ and thus is of compact size. It has omnidirectional properties. The measured gain of this antenna is around 0.5 dB at 2.4 GHz and 1.7 dB at 5 GHz. Its radiation efficiency is greater than 90% in the two frequency bands.

3.3 Baseband Module

Before being implemented in FPGA, the operation of the entire baseband system is simulated in ITPP [15]. Having many toolboxes, ITPP resembles MATLAB, however being in C++ it is better suited to alternate number representations such as integer types. This helps the eventual implementation in FPGA. These concern the issues such as synchronization, accurate channel estimation and packet detection.

3.4 Results Visualization

Following a successful verification of operation of the baseband module via simulations is the FPGA implementation and testing. Experiments concerning the FPGA are accompanied by visualization of the obtained results. These results can also be exported for further processing. Visualization is accomplished through the use of a NIOS II soft-core processor which runs uCLinux and an embedded web server. uCLinux is selected due to its robust and high performance networking capability. On a normal browser, an interface for the results is displayed over HTTP using scalable vector graphics (SVG). On this interface various signal transmission stages can be shown including the time domain signal, the received signal constellation, the decoded signal constellation and the estimated channel matrices. Data of 10ms duration can be displayed every 60–100ms. Fig. 4 and 5 demonstrate visualization capabilities of the UQ MIMO testbed. Fig. 4 illustrates the channel matrix estimation process. In turn, Fig. 5 shows the received (before ML decoding) and decoded signal constellation.

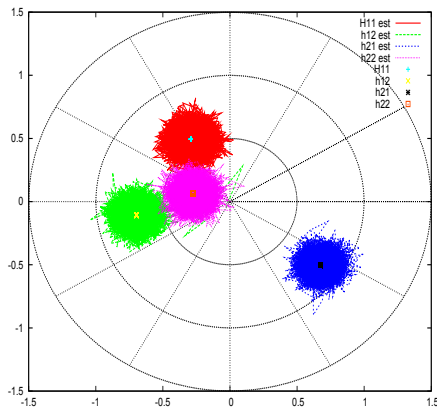


Figure 4: Illustration of channel matrix estimation process for SNR=6dB.

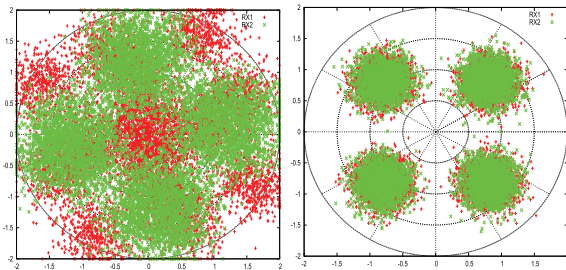


Figure 5: Received and decoded signal constellation.

The presented results confirm the proper operation of the FPGA baseband module and its processing algorithms.

4 CONCLUSIONS

This paper has reported on the design and development of a 2x2 MIMO testbed which uses a Field Programmable Gate Array for parallel processing of baseband signals and commercially available RF transceiver chips and in-house developed antennas in RF front ends. So far, its operation has been investigated using a channel emulator, for both fixed and fading signal cases, assuming QPSK modulation, Alamouti coding scheme and training-based and semi-blind channel estimation methods. These experiments have shown that the developed testbed functions properly.

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